ABSTRACT

A method for making a twin MONOS memory array is described where two nitride storage sites lay under the memory cell word gate. The fabrication techniques incorporate self alignment techniques to produce a small cell in which N+ diffusion the nitride storage sites are defined by sidewalls. The memory cell is used in an NAND array where the memory operations are controlled by voltages on the word lines and column selectors. Each storage site within the memory cell is separately programmed and read by application of voltages to the selected cell through the selected word line whereas the unselected word lines are used to pass drain and source voltages to the selected cell from upper and lower column voltages.